1. A method of forming an embedded ROM product through a selective use of an embedded flash/EEPROM process comprising the steps of:

performing programming simulation for a ROM product using said embedded flash/EEPROM;

generating data to form ROM code for said ROM product;

providing an embedded ROM product substrate having a cell region and a periphery region;

forming a ROM mask;

performing ROM code implant;

forming active devices in said substrate;

forming insulator and metal layer over said devices; and

forming insulator and contact layer over said metal layer.

2. The method of claim 1, wherein said programming simulation is accomplished by using an embedded flash/EEPROM product.

3. The method of claim 1, wherein said ROM mask is for threshold voltage implanting said ROM product.

4. A method of forming a ROM product through a selective use of an embedded flash/EEPROM process comprising the steps of:

providing an embedded flash/EEPROM prototype substrate having different well regions;

defining a cell region and a periphery region further comprising a low-voltage LV-region, and a high-voltage HV-region in said substrate;

forming a gate oxide layer on said substrate including over said cell region and said periphery region;

depositing a first polysilicon layer over said gate oxide layer on said substrate;

forming a nitride layer over said first polysilicon layer;

patterning said nitride layer to form openings to expose portions of said polysilicon layer;

oxidizing said portions of said first polysilicon layer to form poly-oxide as caps over said polysilicon layer;

removing said nitride layer to expose other portions of said first polysilicon layer not protected by said caps;

removing said other portions of said first polysilicon layer by using said poly-oxide as a hard-mask to form floating gate underlying said cap;

forming a first thick interpoly oxide over said substrate, including over said cell region and over said periphery region;

removing said first thick interpoly oxide (IPO) over said periphery LV-region using one photo-mask;

forming a second interpoly low-voltage LV-oxide over said cell region and over said periphery region;

forming a second polysilicon layer over said LV-oxide and said thick interpoly oxide over said substrate, including said cell region and said periphery region;

patterning said second polysilicon layer to form a control gate over said cell region and a poly gate over said periphery region;

performing a lightly doped drain (LDD) implant over said substrate;

forming oxide/SiN spacers along every exposed polysilicon edge, including sides of said floating gate, control gate and gate poly;

performing source/drain implant;

forming an interlevel dielectric layer (ILD) over said substrate;

planarizing said ILD layer using either etch-back or CMP methods;

forming a contact hole in said ILD layer;

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forming metal in said contact hole and continuing to finish said embedded flash/EEPROM memory prototype;

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performing programming simulation for a ROM product using said embedded flash/EEPROM prototype;

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generating data to form ROM code for said ROM product;

75 providing a ROM product substrate having a cell region and a periphery region;

78 forming a ROM gate oxide, comprising LV-gate oxide, over said ROM product substrate, including said cell region and said periphery region;

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forming a gate polysilicon layer over said ROM gate oxide layer;

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patterning said gate polysilicon layer to form a polysilicon gate;

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performing an LDD implant over said ROM substrate;

forming oxide/SiN spacers along sides of said polysilicon gate;

performing source/drain implant over said ROM substrate;

forming a ROM mask;

performing ROM code implant, using said ROM mask;

forming an ILD layer over said substrate;

forming a contact hole in said ILD layer; and

forming metal in said contact hole to and continuing to complete the said flash ROM product.

5. The method of claim 4, wherein said well regions are N-type and P-type.

6. The method of claim 4, wherein said forming said floating gate oxide layer is accomplished by thermal oxidation at a temperature between about 800 to 1000 °C.

7. The method of claim 4, wherein said gate oxide layer has a thickness between about 80 to 120 Å.

8. The method of claim 4, wherein said depositing a first polysilicon layer is accomplished by LPCVD method employing silane SiH_4 as a silicon source material at a temperature range between about 550 to 650 °C.

9. The method of claim 4, wherein said first polysilicon layer has a thickness between about 1000 to 2000 Å.

10. The method of claim 4, wherein said nitride layer has a thickness between about 800 to 2000 Å.

11. The method of claim 4, wherein said oxidizing said portions of said polysilicon layer to form said poly-oxide caps is accomplished by wet oxidation at a temperature between about 800 to 1000 °C.

12. The method of claim 4, wherein said forming a first interpoly oxide layer is accomplished at a temperature between about 700 to 1000 °C.

13. The method of claim 4, wherein said first interpoly oxide is ONO and has a thickness between about 150 to 300 Å.

14. The method of claim 4, wherein said forming a second interpoly oxide layer is accomplished by thermal growth at a temperature between about 800 to 1000 °C.

15. The method of claim 4, wherein said second interpoly oxide is ONO having a thickness between about 30 to 150 Å.

16. The method of claim 4, wherein said forming said second polysilicon layer is accomplished by LPCVD method employing silane SiH_4 as a silicon source material at a temperature range between about 550 to 650 °C.

17. The method of claim 4, wherein said second polysilicon layer is silicided to include WSi_x, $TiSi_x$, or Si_x to form a polycide layer.

18. The method of claim 17, wherein said polycide layer has a thickness between about 2000 to 3000 Å.

19. The method of claim 4, wherein said ONO spacers have a thickness between about 800 to 2000 Å.

20. The method of claim 4, wherein said performing said source/drain implant is accomplished with ions As/P or B/BF_2 at a dosage between about $1x10^{15}$ to $5x10^{15}$ atoms/cm^2 and at an energy between about 20 to 50 KEV.

21. The method of claim 4, wherein said performing said ROM code implant is accomplished with boron (B) ions at a dosage between about $1x10^6$ to $3x10^6$ atoms/cm^2 and at an energy between about 100 to 200 KEV.

22. The method of claim 4, wherein said ILD layer has a thickness between about 7000 to 14000 Å.

23. The method of claim 4, wherein said metal is Al or Cu having a thickness between about 4000 to 6000 Å.

24. The method of claim 4, wherein said performing said programming simulation for a ROM product is accomplished by using threshold voltage implant method.

25. The method of claim 4, wherein said ROM gate oxide has a thickness between about 30 to 150 Å.

26. The method of claim 4, wherein said gate polysilicon layer is silicided to have a total thickness between about 2000 to 3000 Å.

27. The method of claim 4, wherein said performing said LDD implant is accomplished as in the embedded flash/EEPROM process.

28. The method of claim 4, wherein said oxide/SiN spacers have a thickness between about 800 to 2000 Å.

29. The method of claim 4, wherein said performing said ROM code implant is accomplished with ions boron at a dosage between about $1x10^6$ to $3x10^6$ atoms/cm^2 and at an energy between about 100 to 200 KEV.

30. The method of claim 4, wherein said forming said contact hole is accomplished by etching said ILD with a recipe comprising CF_4.

31. The method of claim 4, wherein said metal is Al or Cu having a thickness between about 4000 to 6000 Å.

32. A method of providing ROM products to a customer, comprising:

providing a first manufacturing process for an embedded Flash or embedded EEPROM product;

manufacturing said embedded Flash or embedded EEPROM product by said first manufacturing process, for said customer's prototyping activities;

providing a second manufacturing process for an embedded ROM product, that is similar to said first manufacturing process;

manufacturing said embedded ROM product by said second manufacturing process, whereby said customer has to do minimal re-design in converting a design of said embedded Flash or embedded EEPROM product to a design of said embedded ROM product.

33. The method of Claim 32, wherein said first manufacturing process comprises:

providing an embedded flash/EEPROM prototype substrate having different well regions;

defining a cell region and a periphery region further comprising a low-voltage LV-region, and a high-voltage HV-region in said substrate;

forming a gate oxide layer on said substrate including over said cell region and said periphery region;

depositing a first polysilicon layer over said gate oxide layer on said substrate;

forming a nitride layer over said first polysilicon layer;

patterning said nitride layer to form openings to expose portions of said polysilicon layer;

oxidizing said portions of said first polysilicon layer to form poly-oxide as caps over said polysilicon layer;

removing said nitride layer to expose other portions of said first polysilicon layer not protected by said caps;

removing said other portions of said first polysilicon layer by using said poly-oxide as a hard-mask to form floating gate underlying said cap;

forming a first thick interpoly oxide over said substrate, including over said cell region and over said periphery region;

removing said first thick interpoly oxide (IPO) over said periphery LV-region using one photo-mask;

forming a second interpoly low-voltage LV-oxide over said cell region and over said periphery region;

forming a second polysilicon layer over said LV-oxide and said thick interpoly oxide over said substrate, including said cell region and said periphery region;

patterning said second polysilicon layer to form a control gate over said cell region and a poly gate over said periphery region;

performing a lightly doped drain (LDD) implant over said substrate;

forming oxide/SiN spacers along every exposed polysilicon edge, including sides of said floating gate, control gate and gate poly;

performing source/drain implant;

forming an interlevel dielectric layer (ILD) over said substrate;

planarizing said ILD layer using either etch-back or CMP methods;

forming a contact hole in said ILD layer; and

forming metal in said contact hole and continuing to finish said embedded flash/EEPROM memory prototype.

34. The method of Claim 32, wherein said second manufacturing process comprises:

providing a ROM product substrate having a cell region and a periphery region;

forming a ROM gate oxide, comprising LV-gate oxide, over said ROM product substrate, including said cell region and said periphery region;

forming a gate polysilicon layer over said ROM gate oxide layer;

patterning said gate polysilicon layer to form a polysilicon gate;

performing an LDD implant over said ROM substrate;

forming oxide/SiN spacers along sides of said polysilicon gate;

performing source/drain implant over said ROM substrate;

forming a ROM mask;

performing ROM code implant, using said ROM mask;

forming an ILD layer over said substrate;

forming a contact hole in said ILD layer; and

forming metal in said contact hole to and continuing to complete the said flash ROM product.

35. The method of claim 32, wherein said second manufacturing process differs from said first manufacturing process in the following way: a high voltage, thick oxide process and a first polysilicon process are not needed since said embedded ROM product does not require a floating gate.

36. The method of claim 32, further comprising the steps of: assisting the customer in said minimal re-design by turning off a high voltage transistor of said embedded Flash or embedded EEPROM product, and disabling program and erase of said embedded Flash or embedded EEPROM product, through a logic operation at mask level.

37. A method of providing ROM products to a customer, comprising:

manufacturing an embedded Flash or embedded EEPROM product by a first manufacturing process, for said customer's prototyping activities;

manufacturing an embedded ROM product by a second manufacturing process that is similar to said first manufacturing process, whereby said customer has to do minimal re-design in converting a design of said embedded Flash or embedded EEPROM product to a design of said embedded ROM product.

38. The method of Claim 37, wherein said first manufacturing process comprises:

providing an embedded flash/EEPROM prototype substrate having different well regions;

defining a cell region and a periphery region further comprising a low-voltage LV-region, and a high-voltage HV-region in said substrate;

forming a gate oxide layer on said substrate including over said cell region and said periphery region;

depositing a first polysilicon layer over said gate oxide layer on said substrate;

forming a nitride layer over said first polysilicon layer;

patterning said nitride layer to form openings to expose portions of said polysilicon layer;

oxidizing said portions of said first polysilicon layer to form poly-oxide as caps over said polysilicon layer;

removing said nitride layer to expose other portions of said first polysilicon layer not protected by said caps;

removing said other portions of said first polysilicon layer by using said poly-oxide as a hard-mask to form floating gate underlying said cap;

forming a first thick interpoly oxide over said substrate, including over said cell region and over said periphery region;

removing said first thick interpoly oxide (IPO) over said periphery LV-region using one photo-mask;

forming a second interpoly low-voltage LV-oxide over said cell region and over said periphery region;

forming a second polysilicon layer over said LV-oxide and said thick interpoly oxide over said substrate, including said cell region and said periphery region;

patterning said second polysilicon layer to form a control gate over said cell region and a poly gate over said periphery region;

performing a lightly doped drain (LDD) implant over said substrate;

forming oxide/SiN spacers along every exposed polysilicon edge, including sides of said floating gate, control gate and gate poly;

performing source/drain implant;

forming an interlevel dielectric layer (ILD) over said substrate;

planarizing said ILD layer using either etch-back or CMP methods;

forming a contact hole in said ILD layer; and

forming metal in said contact hole and continuing to finish said embedded flash/EEPROM memory prototype.

39. The method of Claim 37, wherein said second manufacturing process comprises:

providing a ROM product substrate having a cell region and a periphery region;

forming a ROM gate oxide, comprising LV-gate oxide, over said ROM product substrate, including said cell region and said periphery region;

forming a gate polysilicon layer over said ROM gate oxide layer;

patterning said gate polysilicon layer to form a polysilicon gate;

performing an LDD implant over said ROM substrate;

forming oxide/SiN spacers along sides of said polysilicon gate;

performing source/drain implant over said ROM substrate;

forming a ROM mask;

performing ROM code implant, using said ROM mask;

forming an ILD layer over said substrate;

forming a contact hole in said ILD layer; and

forming metal in said contact hole to and continuing to complete the said flash ROM product.

40. The method of claim 37, wherein said second manufacturing process differs from said first manufacturing process in the following way: a high voltage, thick oxide

process and a first polysilicon process are not needed since said embedded ROM product does not require a floating gate.

41. The method of claim 32, further comprising the steps of: assisting the customer in said minimal re-design by turning off a high voltage transistor of said embedded Flash or embedded EEPROM product, and disabling program and erase of said embedded Flash or embedded EEPROM product, through a logic operation at mask level.

42. A method of providing ROM products to a customer, comprising:

manufacturing an embedded Flash or embedded EEPROM product by a first manufacturing process, for said customer's prototyping activities; manufacturing an embedded ROM product by a second manufacturing process that is similar to said first manufacturing process;, whereby said customer has to do minimal re-design in converting a design of said embedded Flash or embedded EEPROM product to a design of said embedded ROM product;

whereby said customer can use said embedded Flash or embedded EEPROM product for prototyping to develop a software program, until a final level of said software program is established; and

coding said embedded ROM product with said final level of said software program

43. A method of providing ROM products to a customer, comprising:

manufacturing an embedded Flash or embedded EEPROM product by a first manufacturing process, for said customer's prototyping activities, wherein said first manufacturing process comprises:

providing an embedded flash/EEPROM prototype substrate having different well regions;

defining a cell region and a periphery region further comprising a low-voltage LV-region, and a high-voltage HV-region in said substrate;

forming a gate oxide layer on said substrate including over said cell region and said periphery region;

depositing a first polysilicon layer over said gate oxide layer on said substrate;

forming a nitride layer over said first polysilicon layer;

patterning said nitride layer to form openings to expose portions of said polysilicon layer;

oxidizing said portions of said first polysilicon layer to form poly-oxide as caps over said polysilicon layer;

removing said nitride layer to expose other portions of said first polysilicon layer not protected by said caps;

removing said other portions of said first polysilicon layer by using said poly-oxide as a hard-mask to form floating gate underlying said cap;

forming a first thick interpoly oxide over said substrate,

including over said cell region and over said periphery region;

removing said first thick interpoly oxide (IPO) over said periphery LV-region using one photo-mask;

forming a second interpoly low-voltage LV-oxide over said cell region and over said periphery region;

forming a second polysilicon layer over said LV-oxide and said thick interpoly oxide over said substrate, including said cell region and said periphery region;

patterning said second polysilicon layer to form a control gate over said cell region and a poly gate over said periphery region;

performing a lightly doped drain (LDD) implant over said substrate;

forming oxide/SiN spacers along every exposed polysilicon edge, including sides of said floating gate, control gate and gate poly;

performing source/drain implant;

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forming an interlevel dielectric layer (ILD) over said substrate;

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planarizing said ILD layer using either etch-back or CMP methods;

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forming a contact hole in said ILD layer;

72 forming metal in said contact hole and continuing to finish said embedded flash/EEPROM memory prototype;

75 manufacturing an embedded ROM product by a second manufacturing process, wherein said second manufacturing process comprises the same steps as said first 78 manufacturing process except that: a high voltage, thick oxide process and a first polysilicon process are not needed since said embedded ROM product does not require a 81 floating gate.